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(11) EP 1 306 896 A1

(12)

EUROPEAN PATENT APPLICATION
published in accordance with Art. 158(3) EPC

(43) Date of publication:

02.05.2003 Bulletin 2003/18

(51) Int.Cl.: H01L 21/324

(21) Application number: 01947887.4

(86) International application number:
PCT/JP01/05887

(22) Date of filing: 06.07.2001

(87) International publication number:
WO 02/007206 (24.01.2002 Gazette 2002/04)

(84) Designated Contracting States:

AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU
MC NL PT SE TR

• TAMATSUKA, Masaro

SHIN-ETSU HANDOTAI CO., LTD.
Annaka-shi, Gunma 379-0196 (JP)

(30) Priority: 13.07.2000 JP 2000212583

• SHINOMIYA, Masaru

SHIN-ETSU HANDOTAI CO., LTD.
Annaka-shi, Gunma 379-0196 (JP)

(71) Applicant: Shin-Etsu Handotai Co., Ltd
Tokyo 100-0005 (JP)

• MATSUMOTO, Yulchi

SHIN-ETSU HANDOTAI CO., LTD.
Annaka-shi, Gunma 379-0196 (JP)

(72) Inventors:

• KOBAYASHI, Norihiko
SHIN-ETSU HANDOTAI CO., LTD.
Annaka-shi, Gunma 379-0196 (JP)

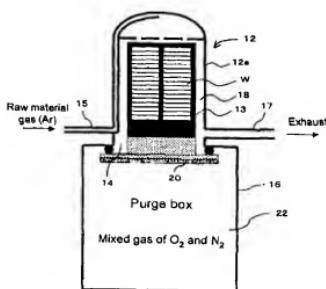
(74) Representative: Grünecker, Kinkeldey,
Stockmair & Schwahnhäuser Anwaltssozietät
Maximilianstrasse 58
80538 München (DE)

• AKIYAMA, Shoji
SHIN-ETSU HANDOTAI CO., LTD.
Annaka-shi, Gunma 379-0196 (JP)

(54) METHOD FOR MANUFACTURING SILICON WAFER

(57) Provided is a process for manufacturing a silicon wafer employing heat treatment which is applied on the silicon wafer in inert gas atmosphere represented by Ar annealing to annihilate Grown-in defects in a surface layer region of the silicon wafer as well as to cause no degradation of haze and micro-roughness on a surface thereof. In a process for manufacturing a silicon wafer having a step of heat treating the silicon wafer in inert gas atmosphere, using a purge box with which the silicon wafer heat treated in the inert gas atmosphere can be unloaded to outside a reaction tube of a heat treatment furnace without being put into contact with the open air, the purge box is filled with mixed gas of nitrogen and oxygen or 100 % oxygen gas, and the heat treated silicon wafer is unloaded into the purge box.

FIG. 1



Description**Technical Field:**

[0001] The present invention relates to a process for manufacturing a silicon wafer (hereinafter also simply referred to as a wafer) employing heat treatment for annihilating Grow-in defects in a surface layer region of the silicon wafer and causing no degradation of haze and micro-roughness on a surface thereof.

Background Art:

[0002] While it has been known that in a CZ silicon wafer there are crystal defects referred to as so called Grow-in defects such as COP (Crystal Originated Particle) and an oxide precipitate, heat treatment performed in hydrogen atmosphere (hereinafter also referred to as hydrogen annealing) has been proposed as a method for annihilating Grow-in defects in the vicinity of a wafer surface. This heat treatment requires use of hydrogen at a high temperature of 1000°C or higher; therefore, a safety measure is required, and an ordinary open furnace (for example, a furnace unsealed on the furnace opening side such as a horizontal furnace) cannot be used for the treatment, so that it is necessary to provide a sealing structure for enhancing air-tightness and an explosion-proof facility as a countermeasure against explosion, resulting in very high cost.

[0003] On the other hand, it has been recently found that the Grow-in defects can be annihilated in heat treatment carried out in argon atmosphere (hereinafter also referred to as Ar annealing) as in the hydrogen annealing. Since the Ar annealing has no explosiveness, a safer operation is ensured as compared with the hydrogen annealing, but it has also been known that the Ar annealing displays a characteristic behavior to a silicon wafer in contrast to the safety operation. There is given as an example of the characteristic behavior a fact that tiny pits are easily formed on a surface of a wafer subjected to the Ar annealing.

[0004] This pit formation is described as follows: An oxide film is formed by oxygen and water as very small amounts of impurities included in raw material gas or oxygen and water in the open air involved through the opening of a reaction tube during a heat treatment step or when unloading a wafer, and the oxide film further reacts with silicon (Si) according to a reaction of $\text{SiO}_2 + \text{Si} \rightarrow 2\text{SiO}$; consequently Si is etched, the etched sites being observed as pits. The pits contribute to degradation of local surface roughness (micro-roughness) and long-periodic surface roughness (haze) on a wafer surface. Thus, Ar gas is sensitive to a trace of impurities, and small environmental changes such as temperature fluctuations, so it has the demerit of difficulty in handling.

[0005] There are proposed the following methods for preventing such degradation of surface roughness of a wafer in the Ar annealing: one is to reduce a water concentration in raw material gas, and the other is to form an etching-resistant film by treating the wafer in oxygen or nitrogen atmosphere prior to unloading it from a heat treatment furnace after the Ar annealing (JP A 93-299413).

[0006] As described in the above published patent application, however, while a nitride film is produced in nitrogen treatment at 1000°C or higher, the nitride film produced at 1000°C or higher has a very slow speed in HF etching, compared with an ordinary natural oxide film, and is not easily etched in cleaning with SC1 (a mixture of $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$), SC2 (a mixture of $\text{HCl}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$) or the like; therefore, it affects heat treatment in the next step. In addition, since a nitride film has a dielectric constant higher than an oxide film, in other word, a higher electrostatic capacitance, charged particles are easy to attach thereto and particles that have been once attached thereto are hard to be removed. This is a drawback when a nitride film is grown on a wafer surface.

[0007] On the other hand, tiny pits are also easily generated when switching Ar gas to oxygen gas prior to unloading a wafer after the Ar annealing. This is because, if oxygen of a prescribed amount or higher is not present in Ar gas (in other words, an oxygen concentration of a prescribed amount or lower), a region where an oxide film is formed is etched by the following reaction:



[0008] This phenomenon inevitably occurs as a transitional one when switching Ar to oxygen. Such etching occurs when a partial pressure of oxygen is a prescribed value or lower even if oxygen is introduced after Ar is removed by a vacuum pump.

55 Disclosure of the Invention:

[0009] There occurs the problem that pits are easily generated by etching when switching Ar gas to oxygen gas not only in Ar annealing but also in annealing using other inert gas atmosphere or inert gas atmosphere including hydrogen

at a content of the explosion limit (4 %) or less (hereinafter simply referred to inert gas atmosphere as a general term). A wafer surface is degraded in terms of haze and micro-roughness the instant that the pits are generated. Moreover, it has been known that the micro-roughness affects an oxide film dielectric breakdown strength and mobility of electrons and holes directly under an oxide film of a transistor of a MOS structure.

5 [0010] Especially, as a drive frequency of a MOS transistor is higher, it is necessary to increase a mobility of carriers (electrons and holes). Furthermore, if a pit is present, concentration of an electric field occurs at the pit; there take place increase in leakage current and degradation in oxide film dielectric breakdown strength. Under these circumstances, it is necessary to reduce the pits of the Ar annealed wafer and improve haze and micro-roughness thereof.

10 [0011] The present invention has been made in view of the problem inherent to the prior art mentioned above, and its object is to provide a process for manufacturing a silicon wafer employing heat treatment for annihilating Grown-in defects in a surface layer region of the silicon wafer causing no degradation of haze and micro-roughness on a surface thereof, the heat treatment being applied on the silicon wafer in inert gas atmosphere represented by Ar annealing.

15 [0012] To solve the problem mentioned above, the present invention provides, in a first aspect, a process for manufacturing a silicon wafer having a step of heat treating the silicon wafer in inert gas atmosphere, wherein using a purge box with which the silicon wafer heat treated in the inert gas atmosphere can be unloaded to outside a reaction tube of a heat treatment furnace without being put into contact with the open air, the purge box is filled with mixed gas of nitrogen and oxygen or 100 % oxygen gas, and the heat treated silicon wafer is loaded into the purge box.

20 [0013] In a second aspect, the present invention provides a process for manufacturing a silicon wafer having a step of heat treating the silicon wafer in inert gas atmosphere, wherein when the silicon wafer heat treated in the inert gas atmosphere is unloaded to outside a reaction tube of a heat treatment furnace, the silicon wafer is unloaded while being blown by mixed gas of nitrogen and oxygen or 100 % oxygen gas.

25 [0014] In a third aspect, the present invention provides a process for manufacturing a silicon wafer having a step of heat treating the silicon wafer in inert gas atmosphere, wherein the heat treatment is performed in a condition that a relationship between an exhaust pressure P (mmHg₂O) and a gas flow rate F (SLM) in a heat treatment furnace during the heat treatment in the inert gas atmosphere satisfies the following equation (1):

$$F \geq (-25/P) + 2.5 \quad (1)$$

30 [0015] The shortest distance between a reaction tube of the heat treatment furnace and the silicon wafer is preferably in the range of from 10 mm to 50 mm. The reason why the upper limit of the shortest distance between the reaction tube and the silicon wafer is 50 mm is that if exceeding 50 mm, a distance between the wafer and the reaction tube (a quartz tube) is excessively large, so the quartz tube having a considerably large inner diameter relative to the wafer to be heat treated is required; there arise too big demerits such as scaling up of an apparatus and low cost-efficiency to be practical.

Brief Description of the Drawings:

[0016]

40 FIG. 1 is a descriptive view showing one embodiment of a first aspect of a process for manufacturing a silicon wafer of the present invention;
 FIG. 2 is a descriptive view showing one embodiment of a second aspect of a process for manufacturing a silicon wafer of the present invention;
 FIG. 3 is a descriptive sectional view showing a positional relationship between a wafer and a quartz tube in one embodiment of a third aspect of a process for manufacturing a silicon wafer of the present invention, wherein part (a) is of a case where the centers of the wafer and the quartz tube are in agreement with each other and part (b) is of a case where the centers are not in agreement with each other;
 FIG. 4 is a graph showing a relationship between an oxygen concentration in mixed gas and haze on a surface of a wafer heat treated in Experimental Example 1;
 FIG. 5 is a graph showing a relationship between an oxygen concentration in mixed gas to be blown against an unloaded wafer and haze on a surface of the heat treated wafer in Experimental Example 2;
 FIG. 6 is a graph showing a relationship between an exhaust pressure P and a gas flow rate F during heat treatment in Experimental Example 3; and
 FIG. 7 is a graph showing a relationship between the shortest distance from a wafer to a quartz tube and haze on a surface of a wafer heat treated in Experimental Example 4.

Best Mode for Carrying Out the Invention:

[0017] Description will be given of embodiments of the present invention below together with the accompanying drawings and it is needless to say that various modifications or alterations in addition to the examples shown in the figures can be performed as far as not departing from the technical concept of the present invention.

[0018] FIG. 1 is a descriptive view showing one embodiment of a first aspect of a process for manufacturing a silicon wafer of the present invention. In FIG. 1, a heat treatment furnace 1 is of a vertical type. The heat treatment furnace 12 has a reaction tube (a quartz tube) 12a, in which many wafers W are disposed in a wafer boat 13. On the side of a furnace opening section 14a a purge box 16 is provided. The purge box 16 is shut off from heat treatment atmosphere 18 during heat treatment of the wafers W. When a shutter 20 at a connecting section is opened in case of unloading the heat treated wafers W, heat treatment atmosphere 18 and atmosphere 22 in the purge box 16 are communicated with each other. The purge box 16 is filled with mixed gas of nitrogen and oxygen before a cover 20 is opened and the heat treated wafers W can be loaded into the purged box 16 filled with the mixed gas atmosphere 22. In FIG. 1, a reference numeral 15 designates a process (raw material) gas supply pipe and a reference numeral 17 designates an exhaust pipe.

[0019] FIG. 2 is a descriptive view showing one embodiment of a second aspect of a process for manufacturing a silicon wafer of the present invention. A heat treatment furnace 12 in FIG. 2 is also of a vertical type. Since a structure of the heat treatment furnace 12 is similar to FIG. 1, the second description thereof is omitted. A gas supply pipe 24 is provided to a furnace opening section 14 of the heat treatment furnace 12 apart from the supply pipe 15 for the process gas (Ar gas). As shown in FIG. 2, while moving the wafer boat 13 downward in order to unload the wafers W, mixed gas 26 is supplied in approximately parallel with a wafer surface from the gas supply pipe 24. With the above construction, invasion of atmospheric air into the heat treatment furnace 12 can be effectively prevented as well as a protective film can be formed on a surface of each of the wafers W.

[0020] FIG. 3 is a descriptive sectional view showing a positional relationship between a wafer and a quartz tube in one embodiment of a third aspect of a process for manufacturing a silicon wafer of the present invention, wherein part (a) is of a case where the centers of the wafer and the quartz tube are in agreement with each other and part (b) is of a case where the centers are not in agreement with each other.

[0021] As described above, a process for manufacturing a silicon wafer of the third aspect of the present invention is to perform heat treatment in a condition that a relationship between an exhaust pressure P (mmH₂O) and a gas flow rate F (SLM) in the heat treatment furnace 12 satisfies the following equation (1):

$$F \cong (-25/P) + 2.5 \quad (1)$$

[0022] Here, as shown in FIG. 3 (a) and (b), it was found that a distance between the outer peripheral end of each of the wafers W supported by the wafer boat 13 and the inner wall of the quartz tube 12a affects a haze level of each of the heat treated wafers W, which is shown as a concrete example in Experimental Example 4 described later.

[0023] As shown in FIG. 3 (a), if a wafer W is set in the almost central portion of the quartz tube 12a, a distance D between the outer peripheral end of the wafer W and the inner wall of the quartz tube 12a is almost equal at any position. On the other hand, if a position of a wafer W set in the quartz tube 12a is displaced (the centers of the wafer W and the quartz tube 12a are displaced from each other), the shortest distance d between the wafer W and the quartz tube can be obtained. By setting the shortest distance d to a value in the range of from 10 mm to 50 mm, degradation of a haze level on the heat treated wafer W can be prevented.

[0024] Moreover, if a method for unloading a wafer in the first or second aspect is applied when the heat treated wafer is unloaded in the third aspect of the present invention, it is more effective for preventing degradation of a haze level on a wafer.

[0025] Subsequently, description will be given of the present invention in a more concrete manner taking up experimental examples.

50 (Experimental Example 1)

[0026] Using silicon mirror wafers having a diameter of 150 mm, a conductivity type of p-type, a crystal axis orientation of <100> and a resistivity of 100 Ω·cm, heat treatment was performed in 100 % argon atmosphere at 1200°C for 60 min. A vertical furnace provided with a purge box similar to FIG. 1 was used.

[0027] In this Experimental Example, an influence on haze was investigated changing the mixing ratio of mixed gas composed of nitrogen and oxygen. In the heat treatment, a flow rate of argon gas was 20 SLM, an exhaust pressure was -5 mmH₂O and an unloading temperature was 800°C.

[0028] Haze measurement was performed with Surfscan SP1 made by KLA-tencor Corp. This measuring instrument

is operated such that a wafer surface is scanned with laser light, a scattered light intensity is measured and the scattered light intensity is obtained in the unit of ppm relative to incident light. The results of the haze measurement are shown in FIG. 4.

[0029] From the results of FIG. 4, it has been found that in mixed gas atmosphere of nitrogen and oxygen or 100 % oxygen atmosphere, a haze level is low, and the lower the oxygen concentration is, the lower the haze level becomes. However, a haze level of a wafer treated with 100 % nitrogen atmosphere when unloading it was extremely high as compared with other conditions.

(Experimental Example 2)

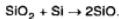
[0030] Instead of the method with the purge box in Experimental Example 1, using a method wherein as shown in FIG. 2 when unloading a wafer a mixed gas stream of oxygen and nitrogen was blown against the got out wafer, such an experiment as Experimental Example 1 was conducted to investigate haze levels of the got out wafers.

[0031] In this Experimental Example, an influence on haze was investigated changing the mixing ratio of mixed gas blown against the unloaded wafer. The results of the haze measurement are shown in FIG. 5.

[0032] From the results of FIG. 5, it has been found that if the blowing gas stream is of mixed gas of nitrogen and oxygen or 100 % oxygen atmosphere, a haze level is low, and the lower the oxygen concentration is, the lower the haze level becomes. However, a haze level of a wafer treated with 100 % nitrogen atmosphere when unloading it was extremely high as compared with other conditions.

[0033] As described above, both of Experimental Examples 1 and 2 showed the phenomenon that in mixed gas of nitrogen and oxygen or 100 % oxygen atmosphere, a haze level is low, and in 100 % nitrogen atmosphere, a haze level is high. The following is considered as the cause of the above phenomenon.

[0034] The reason why tiny pits are easy to occur when switching the gas from Ar gas to oxygen gas before unloading the Ar annealed wafer is that since oxygen of a prescribed amount or more is not present in Ar gas as described above, in a region where an oxide film is formed the following reaction occurs to etch the region:



[0035] This phenomenon inevitably occurs as a transitional one when switching the gas from Ar to oxygen. Therefore, it is estimated that as in the Experimental Examples 1 and 2, using a method wherein a wafer is loaded directly into the atmosphere containing oxygen of a certain concentration (a partial pressure) with the purge box or another method wherein a gas stream containing oxygen is directly blown against a wafer, a sufficient protective oxide film is formed by oxygen gas at a certain partial pressure; therefore, a haze level is effectively reduced, while using 100 % nitrogen atmosphere instead of the above atmosphere, a nitride film as a protective film is insufficiently formed because of an unloading temperature of 800°C and water as a trace of impurity included in the nitrogen gas causes the above reaction locally; a haze level is degraded in this Experimental Example. Furthermore, when an oxygen concentration of mixed gas atmosphere of nitrogen and oxygen is less than 1 %, it has been experimentally confirmed that while degradation in haze level does not occur sometimes, there increase variations in haze level on a wafer and between heat treated batches. Therefore, an oxygen concentration in mixed gas atmosphere is preferably 1 % or higher.

(Experimental Example 3)

[0036] Using silicon mirror wafers having a diameter of 150 mm, a conductivity type of p-type, a crystal axis orientation of < 100 > and a resistivity of 10 Ω·cm, heat treatment was performed in 100 % argon atmosphere at 1200°C for 60 min, a gas flow rate and an exhaust pressure in the heat treatment having been changed. There was used a heat treatment furnace of a general vertical type and the loading and unloading temperature of a wafer was 600°C. An inner diameter of a quartz tube of the used heat treatment furnace is 220 mm and a wafer is set so as to be in the central portion thereof.

[0037] An exhaust pressure during the heat treatment is defined as a pressure differential (a pressure differential relative to the atmospheric pressure) between a pressure sensor installed in the vicinity of an exhaust port of the furnace and a pressure sensor installed outside the furnace. As the experimental conditions, a gas flow rate F was set in the range of from 3 to 30 (SLM) and an exhaust pressure P was set in the range of from - 5 to - 25 (mmH₂O). Note that 1 SLM (Standard Liter per Minute) designates a flow rate when a gas of 1 liter in the standard condition flows for 1 min.

[0038] The heat treated wafer was observed under the collimated light and a haze level was investigated according to whether or not cloudiness was observed in a peripheral portion of the wafer. The results of the investigation are shown in Table 1. In addition, the results in Table 1 were plotted to make a graph to obtain a boundary line between

the presence or absence of cloudiness in the peripheral portion, with the finding that the boundary line is expressed approximately by the following equation (Fig. 6):

$$F = (-25/P) + 2.5.$$

[0039] Note that while the reason why a difference in occurrence of the cloudiness in the wafer peripheral portion exists according to a relationship between a gas flow rate and an exhaust pressure is not clear, it is considered that a gas flow in the vicinity of the wafer peripheral portion affects pit formation due to etching. That is, it is estimated that if a negative pressure of an exhaust pressure relative to the atmospheric pressure becomes higher, a gas flow smoothes even at a smaller gas flow rate, while if the negative pressure is low, gas is apt to be stagnant in a vortex in the vicinity of the peripheral portions between the wafers unless a gas flow rate is increased to a certain extent; therefore, pits are easily formed only in the wafer peripheral portion.

Table 1

		Evaluation by observation in Table 1 is defined as follows:				
		Exhaust pressure P (mmH ₂ O)				
		-25	-20	-15	-10	-5
Gas flow rate F (SLM)	3	×	×	×	×	×
	5	○	○	○	○	×
	10	○	○	○	○	○
	20	—	—	○	○	○
	30	—	—	—	—	○

○ ; no cloudiness in the peripheral portion, X ; occurrence of cloudiness in the peripheral portion, and — ; no experiment performed

(Experimental Example 4)

[0040] Two parameter values $F = 10 \text{ SLM}$ and $P = -15 \text{ mmH}_2\text{O}$ were selected among combinations of the exhaust pressures P and the gas flow rates F in Table 1 of Experimental Example 3 and a relationship between the shortest distance from a wafer to a quartz tube and a haze level was investigated. Specifically, since in Experimental Example 3, a wafer was set almost in the central portion of a quartz tube, a distance D between an outer peripheral end of the wafer and an inner wall of the quartz tube was almost uniformly 35 mm at any point as shown in FIG. 3(a), while in this Experimental Example, a position at which a wafer was set in the quartz tube was displaced (the centers of the wafer and the quartz tube was displaced from each other) to thereby change the shortest distance d between the wafer and the quartz tube in the range of from about 2.5 to 30 mm. Under the various shortest distances the wafers were heat treated. Haze levels on the heat treated wafers were investigated. The results of the investigation are shown in FIG. 7.

[0041] From the results of FIG. 7, it has been found that a haze level on the heat treated wafer is related to the shortest distance between the wafer and the quartz tube and the haze level on the wafer is extremely degraded at the distance of 10 mm or less. While a cause of this phenomenon is not clear, it is expected that a gas flow in the vicinity of a wafer peripheral portion exerts an effect on pit formation due to etching as in Experimental Example 3.

Capability of Exploitation in Industry:

[0042] As described above, according to the present invention, an effect can be achieved that heat treatment in inert gas atmosphere represented by Ar annealing is applied on a silicon wafer to annihilate Grown-in defects in a wafer surface layer region as well as to cause no degradation of haze and micro-roughness on a surface thereof.

Claims

1. A process for manufacturing a silicon wafer having a step of heat treating the silicon wafer in inert gas atmosphere, wherein using a purge box with which the silicon wafer heat treated in the inert gas atmosphere can be unloaded to outside a reaction tube of a heat treatment furnace without being put into contact with the open air, the purge

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box is filled with mixed gas of nitrogen and oxygen or 100 % oxygen gas, and the heat treated silicon wafer is loaded into the purge box.

5 2. A process for manufacturing a silicon wafer having a step of heat treating the silicon wafer in inert gas atmosphere, wherein when the silicon wafer heat treated in the inert gas atmosphere is unloaded to outside a reaction tube of a heat treatment furnace, the silicon wafer is unloaded while being blown by mixed gas of nitrogen and oxygen or 100 % oxygen gas.

10 3. A process for manufacturing a silicon wafer having a step of heat treating the silicon wafer in inert gas atmosphere, wherein in the heat treatment is performed in a condition that a relationship between an exhaust pressure P (mmH_2O) and a gas flow rate F (SLM) in a heat treatment furnace during the heat treatment in the inert gas atmosphere satisfies the following equation:

$$F \geq (-25/P) + 2.5 \quad (1)$$

4. A process for manufacturing a silicon wafer according to claim 3, wherein in the heat treatment, the shortest distance between a reaction tube of the heat treatment furnace and the silicon wafer is in the range of from 10 mm to 50 mm.

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FIG. 1

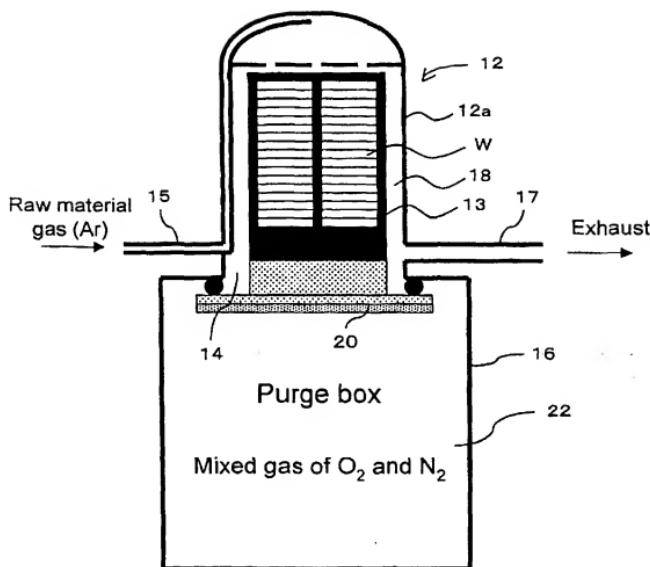
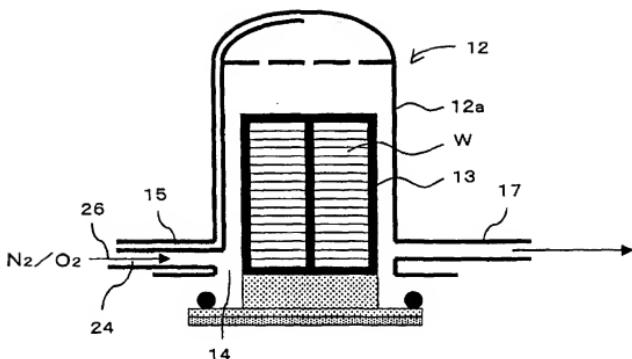


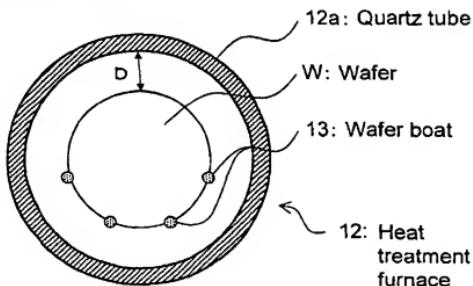
FIG. 2



N_2 and O_2 are blown while moving boat downward

FIG. 3

(a) Centers of wafer and quartz tube are in agreement with each other



(b) Centers of wafer and quartz tube are not in agreement with each other

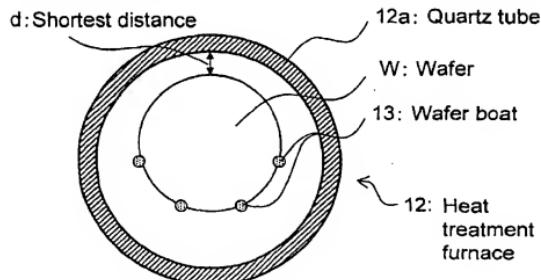


FIG. 4

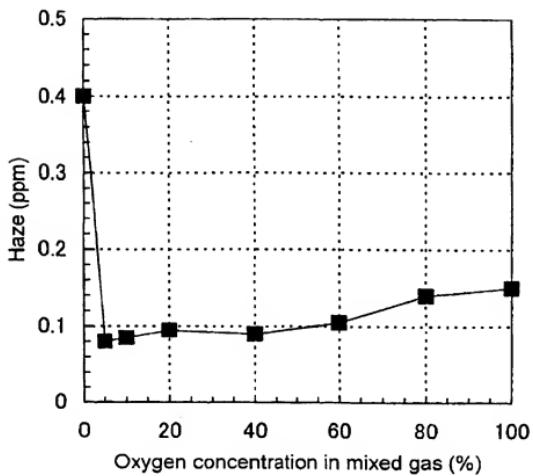


FIG. 5

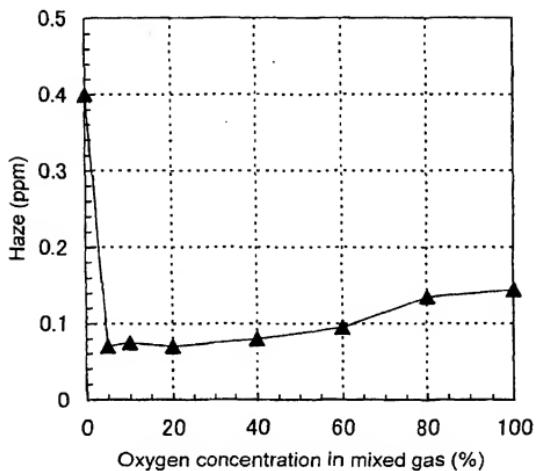


FIG. 6

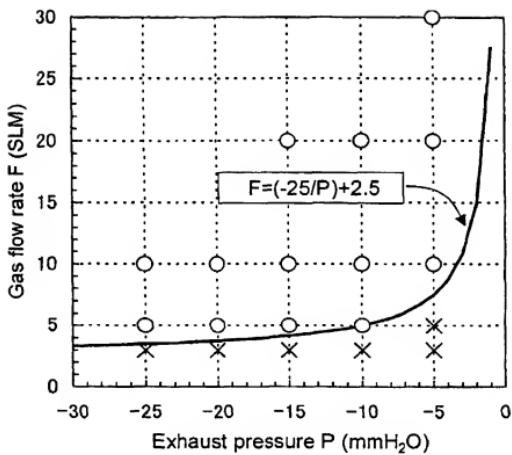
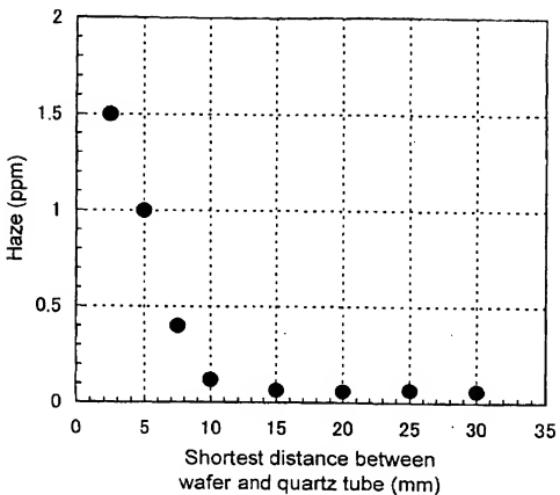


FIG. 7



INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP01/05887

A. CLASSIFICATION OF SUBJECT MATTER Int. Cl ⁷ H01L21/324		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) Int. Cl ⁷ H01L21/00, H01L21/22-21/24, H01L21/26-21/268, H01L21/322-21/326, H01L21/205, H01L21/31, H01L21/312-21/32, H01L21/58		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Jitsuyo Shinan Kobo 1922-1996 Toroku Jitsuyo Shinan Kobo 1994-2001 Kokai Jitsuyo Shinan Kobo 1971-2001 Jitsuyo Shinan Toroku Kobo 1996-2001		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category ⁸	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 5-299413 A (Toshiba Corporation), 12 November, 1993 (12.11.93), Full text; Figs. 1 to 6 (Family: none)	1, 2
A	JP 4-62840 A (Kawasaki Steel Corporation), 27 February, 1992 (27.02.92), Full text; Figs. 1 to 4 (Family: none)	1, 2
A	US 5735961 A (Kokusai Electric Co., Ltd.), 07 April, 1998 (07.04.98), Full text; Figs. 1 to 5 & JP 9-45597 A Full text; Figs. 1 to 5 & TW 322590 A & US 5879415 A & KR 245259 A	1, 2
A	JP 2000-174028 A (Kogyo Thermal System K.K.), 23 June, 2000 (23.06.00), Full text; Figs. 1 to 2 (Family: none)	1, 2
<input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
<p>* Special categories of cited documents:</p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance;</p> <p>"E" document not published on or after the international filing date</p> <p>"I" document which may throw doubt on priority claim(s) or which is cited to establish the publication date of another citation, or other relevant reason (as specified);</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed.</p>		<p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document which is not published on or after the international filing date and which cannot be considered novel, or cannot be considered to involve an inventive step when the document is taken alone</p> <p>"Y" document of particular relevance when the claimed invention cannot be considered novel, or cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</p> <p>"G" document member of the same patent family</p>
Date of the actual completion of the international search 12 September, 2001 (12.09.01)	Date of mailing of the international search report 25 September, 2001 (25.09.01)	
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer	
Faxsimile No.	Telephone No.	

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP01/05887

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 5-82460 A (Fujiitsu Limited), 02 April, 1993 (02.04.93), Full text; Figs. 1 to 2 (Family: none)	2
A	JP 5-291269 A (Nippon Steel Corporation), 05 November, 1993 (05.11.93), Full text; Fig. 1 (Family: none)	2
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